

## ABSTRACT OF THE DISCLOSURE

The present invention is used for guiding formal verification of a circuit design in circuit simulation software to optimize the time required for verification of a circuit design. The invention modifies the analysis region being used for verification in order to optimize the time for verification. The invention allows for manual, semi-automatic, and automatic modification of the analysis region. The modification is done by either expanding or reducing the analysis region or by adding new rules as assumptions to the existing analysis region. The invention also uses the concept of an articulation point for modification of the analysis region. The modification of the analysis region is performed in a manner to optimize time and memory required for verification of the circuit design.